**QUESTION#5**

TRUE/FALSE

1. A latch has one stable state. **(FALSE)**

2. A latch is considered to be in the RESET state when the Q output is low. **(TRUE)**

3. A gated D latch cannot be used to change state. **(FALSE)**

4. Flip-flops and latches are both bi stable devices. **(TRUE)**

5. An edge-triggered D flip-flop changes state whenever the D input changes. **(FALSE)**

6. A clock input is necessary for an edge-triggered flip-flop. **(TRUE)**

7. When both the J and K inputs are HIGH, an edge-triggered J-K flip-flop changes state on each Clock pulse. **(TRUE)**

**QUESTION#6**

MCQS

1. A flip-flop changes its state during the

(a) Complete operational cycle

(b) Falling edge of the clock pulse

(c) Rising edge of the clock pulse

(d) Both answers (b) and (c)

2. The purpose of the clock input to a flip-flop is to

(a) Clear the device (b) set the device

(c) Always cause the output to change states

(d) Cause the output to assume a state dependent on the controlling (J-K or D) inputs.

3. for an edge-triggered D flip-flop,

(a) A change in the state of the flip-flop can occur only at a clock pulse edge

(b) The state that the flip-flop goes to depends on the D input

(c) The output follows the input at each clock pulse

(d) All of these answer

4. A feature that distinguishes the J-K flip-flop from the D flip-flop is the

(a) Toggle condition

(b) preset input

(c) Type of clock

(d) Clear input

5. A flip-flop is SET when

(a) J = 0, K = 0

(b) J = 0, K = 1

(c) J = 1, K = 0

(d) J = 1, K = 1

(e) D = HIGH, EN = HIGH

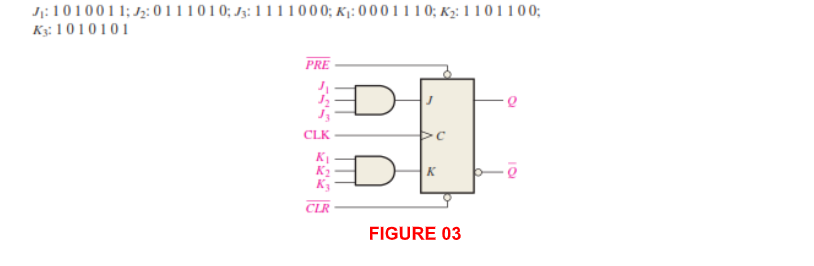
**QUESTION#7**

The following serial data are applied to the flip-flop through the AND gates as indicated in

Figure 03. Determine the resulting serial data that appear on the Q output. There is one

Clock pulse for each bit time. Assume that Q is initially 0 and that PRE and CLR are HIGH.

Rightmost bits are applied first.



**ANSWER:**

**Q=1111011**

